

Description**BACKGROUND OF THE INVENTION**5 **Field of the Invention**

[0001] The present invention relates to a heat treatment apparatus and a heat treatment method for heat-treating a semiconductor article in production of a semiconductor device for integrated circuits. The present invention also relates to a process for producing a semiconductor article.

10 **Related Background Art**

[0002] In production of a semiconductor device, a heat treatment apparatus is used in a process of forming an oxide film, or diffusing an impurity as a donor or an acceptor, and in a process of annealing a semiconductor article such as a bulk Si wafer in a hydrogen-containing reducing atmosphere.

[0003] Fig. 9 shows a first example of heat treatment apparatuses of prior arts. This heat treatment apparatus has inner tube 1 and outer tube 2. A hydrogen-containing reducing gas G_H is introduced from inlet 5, and is discharged through vent 6. Into the interspace between inner tube 1 and outer tube 2, an oxygen-containing gas G_O is introduced through inlet 7 and is discharged through vent 8 to prevent penetration of copper (Cu) from the outside into inner tube 1. The symbol W indicates an Si wafer. The numeral 4 indicates a boat. Such an apparatus is disclosed in Japanese Patent Application Laid-Open No. 5-152309.

[0004] Fig. 10 shows a second example of heat treatment apparatuses of prior arts. This heat treatment apparatus comprises inner tube 1 made of silicon carbide (SiC), heater 3, and therebetween an open-ended outer tube 2 made of fused quartz produced by an oxyhydrogen flame fusion method and containing OH groups at a content of 200 ppm. The outer tube prevents diffusion of metal impurity. Such an apparatus is disclosed in Japanese Patent Application Laid-Open No. 7-193074.

[0005] Fig. 11 shows a third example of heat treatment apparatuses of prior arts. This heat treatment apparatus comprises inner tube 1 made of SiC, and outer tube 2 made of fused quartz. An oxygen-containing purge gas is introduced into the interspace between inner tube 1 and outer tube 2 through inlet pipe 7 and is discharged through vent pipe 8. A cooling gas is introduced through inlet pipe 10 and is discharged through vent pipe 11. The numeral 9 indicates a table which serves as a heat barrier. Such an apparatus is disclosed in Japanese Patent Application Laid-Open No. 8-31761.

[0006] Fig. 12 shows a fourth example of heat treatment apparatuses of prior arts. This heat treatment apparatus comprises inner tube 1 and outer tube 2, both made of fused quartz, and heat equalizer tube 20 between outer tube 2 and heater 3. An oxygen-containing gas is introduced from gas inlet pipe 12 at the bottom to the interspace between inner tube 1 and outer tube 2, further introduced to the inside of inner tube 1 through plural gas inlet holes 5, and discharged from vent pipe 6. The numeral 13 indicates a heat insulating material. Such an apparatus is disclosed in Japanese Patent Application Laid-Open No. 7-161655.

[0007] Fig. 13 shows a fifth example of heat treatment apparatus of prior arts. This apparatus comprises inner tube 1 made of SiC, and outer tube 2 made of fused quartz. A treating gas like an oxidizing gas is introduced from inlet 5 at the bottom into inner tube 1, further introduced through communication hole 13 into the interspace between inner tube 1 and outer tube 2, and discharged from vent 6. Such an apparatus is disclosed in Japanese Patent Application Laid-Open No. 7-302767.

[0008] However, the apparatuses of the prior arts have problems of contamination, treating gas leakage, reaction tube deformation, reaction tube cracking, and so forth, which have not been solved.

[0009] On the other hand, it was found by the inventors of the present invention that, in heat treatment in hydrogen-containing reducing atmosphere, semiconductor articles are etched undesirably.

SUMMARY OF THE INVENTION

[0010] An object of the present invention is to provide a heat treatment apparatus, a heat treatment method, and production process for semiconductor articles, in which the metal contamination caused by the metal of a reaction tube is reduced.

[0011] Another object of the present invention is to provide a heat treatment apparatus, a heat treatment method, and production process for semiconductor articles, in which gas leakage caused by reaction tube deformation is prevented.

[0012] A further object of the present invention is to provide a heat treatment apparatus, a heat treatment method, and production process for semiconductor articles, in which undesired etching is prevented.

[0013] According to an aspect of the present invention, there is provided a heat treatment apparatus which comprises a first tube, a second tube placed therein, and a heater, wherein the first tube is lightly closable and is made of vitreous silica having an impact strength higher than that of the second tube, the second tube has at least an internal face comprised of non-silicon oxide, and a gas flow path is constructed to introduce a gas into a treatment space in the second tube without passing over a face comprised of silicon oxide heated to a high temperature by the heater.

[0014] According to another aspect of the present invention, there is provided a heat treatment apparatus comprising a first tube, a second tube placed therein, and a heater, wherein a gas inlet for introducing the gas in the second tube is provided below the heater, a hole for communicating the first tube to the second tube is provided at a top portion of the second tube, a vent is provided at a bottom portion of the first tube for discharging the gas from inside of the first tube, the first tube is constructed from fused quartz and is closable, the second tube has a non-silicon oxide surface and is closable, and the heater is provided at a higher level than a heat barrier placed in the second tube.

[0015] According to another aspect of the present invention, there is provided a heat treatment process for heat-treating a semiconductor article by means of the heat treatment apparatuses set forth in above.

[0016] According to a further aspect of the present invention, there is provided a process for producing a semiconductor article, the process comprising bonding a first base plate and a second base plate, eliminating an unnecessary portion of the first base member from the second base member, and heat-treating a silicon body on the second base member in a hydrogen-containing reducing atmosphere by means of the above-mentioned treatment apparatuses set forth in above.

20 BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Fig. 1 is a sectional view of an example of a heat treatment apparatus of the present invention.

[0018] Fig. 2 is a sectional view of a heat treatment apparatus.

[0019] Fig. 3 is a sectional view of the heat treatment apparatus of a second embodiment of the present invention.

[0020] Fig. 4 is a sectional view of the heat treatment apparatus of a third embodiment of the present invention.

[0021] Fig. 5 is a sectional view of the heat treatment apparatus of a fourth embodiment of the present invention.

[0022] Fig. 6 is a sectional view of the heat treatment apparatus of a fifth embodiment of the present invention.

[0023] Fig. 7 is a flow chart of the process of producing a semiconductor article according to the present invention.

[0024] Figs. 8A, 8B, 8C, 8D, 8E and 8F show schematically an embodiment of the process for producing a semiconductor article according to the present invention.

[0025] Fig. 9 is a sectional view of a first example of conventional heat treatment apparatuses.

[0026] Fig. 10 is a sectional view of a second example of conventional heat treatment apparatuses.

[0027] Fig. 11 is a sectional view of a third example of conventional heat treatment apparatuses.

[0028] Fig. 12 is a sectional view of a fourth example of conventional heat treatment apparatuses.

[0029] Fig. 13 is a sectional view of a fifth example of conventional heat treatment apparatuses.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Fig. 1 shows an embodiment of the heat treatment apparatus of the present invention. The heat treatment apparatus has inner tube (second tube) 31, furnace tube (first tube) 32, and hydrogen-containing gas introduction pipe 33. Inner tube 31, and has at least an inside wall comprised of a non-silicon oxide such as silicon carbide, silicon nitride, boron nitride, aluminum oxide etc. Furnace tube 32 is made of impact resistant vitreous silica such as fused quartz. Gas introduction pipe 33 has an inner face comprised of non-silicon oxide similarly as inner tube 31. Heater 3 is placed with the top end at level 51 and the bottom end at level 52 to heat region 50 to a prescribed temperature.

[0031] The hydrogen-containing gas is introduced from inlet 5 into the apparatus, released from outlet 34 to treatment region (treatment space) 54, and discharged through vent 6 at the bottom of the apparatus to the outside. Even if a metallic impurity is emitted from heater 3 or furnace tube 32, the impurity is blocked by inner tube 31 having an inside wall of non-silicon oxide not to reach semiconductor article W. Gas introduction pipe 33 has also an inside wall of non-silicon oxide to prevent emission of metallic impurity into the hydrogen-containing gas in the gas introduction pipe. Metallic impurity may penetrate into region 53, but it will be driven out from vent 6.

[0032] Furnace tube 32 which is made of fused quartz has impact strength higher than inner tube 31, deforms less, and causes difficultly cracking. The impact strength may be thermal impact strength and/or mechanical impact strength. Treatment region 54 is enclosed by inner tube 31 made of heat insulating fused quartz.

[0033] The hydrogen-containing gas is introduced into treatment space 54 in inner tube 31 without passing over a heated silicon oxide face (e.g., region 53) heated by heater 3 to a high temperature.

[0034] The numeral 22 indicates a mount of inner tube 31, the numerals 24 and 25 indicate a sealing member such as an O-ring, the numeral 27 indicates a vent of inner tube 31, and the numeral 26 indicates a furnace cover.

[0035] In the process of heat treatment of a semiconductor article in a hydrogen-containing atmosphere (hydrogen

annealing), etching was found to occur by the inventors of the present invention. This etching is described below. [0036] The detail of the hydrogen annealing is shown, for example, in Japanese Patent Application Laid-Open Nos. 5-218053, and 5-217821; and N.Sato and T.Yonehara: Appl. Phys. Lett. 65 (1994) p.1924.

[0037] Firstly, the inventors of the present invention annealed a substrate of SOI (semiconductor on insulator) in a hydrogen atmosphere with the apparatus shown in Fig. 2.

[0038] In Fig. 2, furnace tube 32 is formed from fused quartz having high heat resistance and high workability. In furnace tube 32, there are placed SOI wafer W to be heat-treated, boat 4 for holding wafer W, and heat barrier 9 for supporting boat 4. Boat 4 is made of a heat-resistant material such as silicon carbide having on the surface an extremely pure SiC coating layer formed by CVD (chemical vapor deposition). Heat barrier 9 is formed from a heat-insulating material such as foamed quartz. Furnace cover 26 seals the opening of furnace tube 32 to be gastight with O-ring 25, and is movable in the direction of arrow mark A by a boat elevator mechanism (not shown in the drawing). Heater 3 heats wafer W by electric current application.

[0039] In this apparatus, the treatment gas is introduced from gas inlet 5 through gas introduction pipe 33 to the top and interior of furnace tube 32. The introduced gas flows in the interior of furnace tube 32 downward, and is discharged through vent 6. The gas inlet 5, gas introduction pipe 33, and vent 6 are usually formed from fused quartz. Setting of wafer W on boat 4 is conducted by lowering furnace cover 26 to such a position that boat 4 is brought out of furnace 32. After setting of the wafer, furnace cover 26 is elevated to insert boat 4 into furnace tube 32 and to close the opening of the furnace tube to be gastight by use of O-ring 25 as shown in Fig. 2. Thereby, the hydrogen gas can be used safely.

[0040] The hydrogen annealing is conducted by introducing a hydrogen gas as the treating gas through gas inlet 5 to replace the internal atmosphere in furnace tube 32 to obtain a hydrogen-containing reducing atmosphere, and applying electric current to a heating resistor of heater 3 to heat wafer W on boat 4 to a prescribed temperature (e.g., 1200°C). After a prescribed time (e.g., one hour), the electric current to the heating resistor is stopped, wafer W is cooled by heat radiation to a prescribed temperature, and simultaneously an inert gas such as nitrogen gas is introduced from gas inlet 5 to replace the hydrogen gas in the furnace tube 32. Then furnace cover 26 is lowered, and wafer W on boat 4 is taken out from furnace tube 32. In such a manner, an SOI substrate is heat-treated in a hydrogen-containing reducing gas atmosphere to flatten and smoothen the surface of the semiconductor body on the substrate.

[0041] In the annealing, the thickness of Si body on the SOI substrate was found to decrease. This is caused by the reaction below. During the hydrogen annealing, the hydrogen gas and the fused quartz reacts to form water.



The formed water, when it reaches the wafer W, reacts with silicon of wafer W to cause etching of silicon.



In treatment of the SOI substrate, this etching decreases the thickness of single crystal silicon layer (SOI layer) on an insulator, and simultaneously causes variation of layer thickness. The variation of the SOI layer thickness deteriorates the properties of the formed electronic device, in particular, of full depletion type of FET (field effect transistor).

[0042] For preventing the etching of silicon, use of silicon carbide which is not reactive to hydrogen gas at a temperature higher than 900°C is effective in place of the fused quartz for the material of furnace tube 32. However, the silicon carbide is brittle to mechanical impact and/or thermal impact, and a silicon carbide furnace tube may cause cracking. Accordingly, the construction and the material of the gas introduction path and the heater should be investigated.

[0043] The fused quartz used for constructing furnace tube 32 contains a metal impurity (e.g., iron) in an amount ranging from about 10 ppm to about 100 ppm by weight. In hydrogen annealing at a temperature of 1000°C or higher, this impurity is released from the fused quartz into the hydrogen gas, and deposits on the surface of wafer W to contaminate it. This metal contamination may shorten the minority carrier lifetime of wafer W, and can deteriorate the performance of the electronic device provided on wafer W.

[0044] In one possible method for prevention of metal contamination, the fused quartz for furnace tube 32 is replaced by silicon carbide which has on the surface a coating layer of extremely pure silicon carbide formed by CVD. However, the silicon carbide which is brittle against mechanical impact and/or thermal impact may cause cracking to leak the hydrogen gas.

[0045] In another method, the fused quartz for furnace tube 32 is replaced by synthetic fused silica which is formed by a direct method. In contrast to the fused quartz produced from a natural mineral resource, the synthetic fused silica is synthesized chemically from SiCl_4 by direct deposition vitrification by oxyhydrogen flame hydrolysis, and contains metal impurity at an extremely low content of 1 ppm by weight or less. However, the synthetic fused silica by a direct method is less heat-resistant than fused quartz. Therefore, furnace tube 32, which is formed from synthetic fused silica,

may cause gas leakage by deformation at a high temperature.

[0046] The heat treatment apparatus shown in Fig. 2, as described above, has disadvantage of metal contamination of wafer W in the hydrogen annealing treatment. Furthermore, the apparatus and the method of Fig. 2 has a disadvantage of etching of silicon by moisture formed by reaction of the hydrogen gas and the fused silica.

[0047] Similarly, in the example shown in Fig. 9, the etching occurs because of absence of an inside liner of non-silicon oxide. In the example shown in Fig. 10, gas leakage is liable to occur since the treatment space is closed by a single tube of SiC. In the example shown in Fig. 11, moisture is developed from table 9 since the top of table 9 made of vitreous silica is heated by heater 3. In the example shown in Fig. 12, etching occurs similarly in hydrogen annealing. In the example shown in Fig. 13 also, water is formed on the top of table 9 constituted of vitreous silica and the gas absorbs the moisture is fed to wafer W to cause etching in hydrogen annealing.

[0048] The present invention solves the problems involved in the conventional apparatuses.

(Embodiment 1)

[0049] A first embodiment of the present invention is described by reference to Fig. 1.

[0050] In this embodiment, furnace tube 32, gas inlet 5, and vent 6 are formed from fused quartz in one body. The boat 4 for holding wafer W is made of silicon carbide, and thereon a coating layer of extremely pure SiC is formed by CVD. Heat barrier 9 is made of heat-insulating foamed silica (porous silicon oxide), and is not heated to a temperature of 1000°C or higher.

[0051] Inner tube 31, which may be called a second furnace tube or an inner liner, is a cylindrical member having an open top end and an open bottom end, and has hole 27 communicating with vent 6 at the bottom portion. Inner tube 31 is made of silicon carbide material, and its inside face is coated with an SiC coating layer formed by CVD. Inner tube mount 22 supports inner tube 31, being movable in the direction shown by arrow mark B (vertical direction) by an inner tube elevator (not shown in the drawing) when the inner tube is mounted or demounted. O-ring 24 ensures gastightness between furnace cover 26 and inner tube mount 22. O-ring 25 ensures gastightness between inner tube mount 22 and furnace tube 32. Pipe 28 introduces the gas from inner tube 31, and allows the gas to flow through hole 27 to vent 6.

[0052] With this constitution, wafer W is treated for hydrogen annealing at a temperature, for example, 1000°C or higher. In the hydrogen annealing, hydrogen gas is introduced through gas inlet 5 and gas introduction pipe 33 into furnace tube 32. A portion of the introduced gas passes through the inside of inner tube 31, and is discharged through pipe 28 and vent 6 to the outside, and the rest of the introduced hydrogen gas passes through the interspace (region 53) between furnace tube 32 and inner tube 31 and is discharged from vent 6.

[0053] Thereby inner tube 31 serves to shield the wafer W from the metallic impurity released from fused quartz of the inside wall of furnace tube 32 and from the moisture formed by reaction between fused quartz of inside wall of furnace tube 32 and the hydrogen gas, which produces the effect of preventing the metal contamination of wafer W and the silicon etching thereof.

[0054] In this embodiment, even if the inner tube 31 is broken or damaged, leakage of the high-temperature hydrogen gas to the outside is prevented by furnace tube 32 surrounding inner tube 31 to be gastight. Therefore, inner tube 31 may be made of a material less resistant to impact and high temperature like SiC without a problem.

[0055] This embodiment has a double tube structure constituted of furnace tube 32 and inner tube 31. Additionally a mantle tube (outer liner) may be provided as a third tube at the outside of furnace tube 32 for intercepting a metallic impurity formed by heater 3 outside furnace tube 32. The mantle tube is preferably made of a material which intercepts effectively the metallic impurity and emits less impurity from the mantle tube itself. An example of the material is silicon carbide having an SiC coating layer formed thereon by CVD.

[0056] In the present invention, silicon carbide coated with SiC by CVD is suitably used as the constituting material for inner tube 31 placed at high-temperature range 50 and for gas introduction tube 33. However, the material is not limited thereto. Any non-silicon oxide material is useful which has a high purity and high heat resistance and does not emit metal in the ambient gas. The useful non-silicon oxide material (non-SiO) includes ceramics such as boron nitride (BN), silicon nitride (SiN), and alumina (Al₂O₃); and silicon. Such a construction material does not emit into the treatment gas an etching substance which etches the surface of the semiconductor material or does not produce an etching substance by reaction with the treatment gas.

[0057] The above "substance which etches the surface of the semiconductor material" etches the semiconductor material by itself or in combination with the ambient gas by reaction with the semiconductor material. The above-mentioned "construction material" itself does naturally not emit the aforementioned etching substance, and further does not form the etching substance by chemical reaction with the ambient gas. The construction material includes a silicon carbide material coated with an SiC film by CVD, and other materials which has high purity, and low chemical activity to the ambient gas, and does not produce moisture by reaction with the ambient gas.

[0058] Inner tube 31 intercepts the wafer W from the etching substance such as moisture formed by reaction of a

silica material with hydrogen in furnace tube 32, and emits by itself no or little amount of an etching substance. Therefore, inner tube 31 serves effectively to reduce the undesired etching of silicon.

[0059] By use of furnace tube 32 made of vitreous silica of high light transmittance, the infrared light emitted by heater 3 is transmitted effectively to wafer W to heat it.

5 [0060] In Fig. 1, the bodies of inner tube 31 and gas introduction pipe 33 are made of SiC. However, they may be made of another material coated with SiC at least on the inside wall of inner tube 31 in high temperature region 50 and on the inside face of gas introduction pipe 33 in high temperature region 50.

10 [0061] The closable or evacuable furnace tube of the present invention is not limited to be made of fused quartz produced by a known process of electric fusion or flame fusion, but may be made of synthetic fused silica produced by a plasma process, a soot process, or a sol-gel process. These vitreous silica, which contains hydroxyl groups at a low content of 300 ppm or lower, has a viscosity coefficient of not less than 10^{11} at 1200°C, thus being resistant to deformation in high-temperature heat treatment.

15 [0062] The third tube, the mantle tube, employed in the present invention may be either of an open type or a closed type. If necessary, a purge gas is allowed to flow through the space between furnace tube 32 and the mantle tube.

15 The mantle tube is necessarily placed in the high temperature region 50.

20 [0063] Heater 3 in the present invention includes those having heating element made of a material such as FeCrAl alloys, Ta alloys, ceramics, and carbon; or halogen lamps, and if necessary, may be provided with heat-conductive equalizer plate additionally.

20 (Embodiment 2)

25 [0064] Embodiment 2 of the present invention is described by reference to Fig. 3. In this embodiment, furnace tube 32, gas inlet 5 at the top of furnace tube 32, and vent 6 are formed in one body from fused quartz. Second furnace tube (inner tube) 31 is cylindrical and capped, having a hole 27 on the side wall at the lower end portion for gas discharge, and having gas introduction pipe 33 at the top. The inside wall of the second furnace tube is coated with SiC by CVD.

30 [0065] In the hydrogen-annealing treatment of wafer W at a high temperature, for example, of 1000°C or higher, the hydrogen gas as the ambient gas is introduced from gas inlet 5 through gas introduction pipe 33 into inner tube 31, and is discharged from hole 27 through vent 6 to the outside.

35 [0066] In this embodiment, the same effect as in Embodiment 1 is achieved. Further, the space in which wafer W is placed is intercepted from the outside by inner tube 31 except the portions in contact with gas introduction pipe 33, hole 27, and furnace cover 26. However, in Embodiment 1, improper adjustment of the gas flow can cause contact of the hydrogen gas with furnace tube 32 to release metallic impurity and produced moisture into the hydrogen gas flow, whereby the gas containing them enters the inside of inner tube 31 to reach wafer W. On the other hand in this embodiment, such a phenomenon does not occur.

40 [0067] This embodiment has a constitution such that the hydrogen gas is not brought into contact with the vitreous silica in the space of wafer W in high-temperature region 50. Therefore, the hydrogen gas in the space where wafer W is placed does not contain metallic impurity released from the vitreous silica or does not contain moisture.

45 [0068] Incidentally, heat barrier 9 and furnace cover 26 are in contact with hydrogen gas in the space where wafer W is placed. However, the contact portions are outside the high temperature region 50 heated by heater 3, not being at a high temperature, so that metallic impurity is not released or moisture is not produced there. Further, in this embodiment, since the hydrogen gas is introduced from gas introduction pipe 33, the hydrogen gas is not brought into contact with the vitreous silica at the upstream region of the hydrogen gas flow relative to wafer W.

45 [0069] This embodiment is summarized as below.

(1) Closed space structure of inner tube:

50 [0070] The space which encloses wafer W is intercepted from the outside by inner tube 31 except for the gas introduction portion (gas introduction pipe 33), the gas-discharging portion (hole 27) and the opening to be closed with furnace cover 26. The wording "space which encloses wafer W" herein means the space occupied by wafer W and the surrounding. The arrangement and the number of the atmospheric gas introduction portions and the atmospheric gas discharging portions are selected suitably without limitation to the description in this embodiment.

55 [0071] Owing to interception of the space enclosing wafer W from the outside, the metallic impurity and moisture released by contact of furnace tube 32 with the hydrogen gas, even if they are released into the hydrogen gas, does not penetrate into the inside of inner tube 31, whereby the contamination by metal and etching of silicon are reduced further.

(2) Prevention of contamination by metal and moisture in closed space:

[0072] The atmospheric gas is not brought into contact with furnace tube 32 in high temperature region 54 of the space enclosing wafer W. The wording "high temperature region 54 of the space enclosing wafer W" herein means a region heated by heater 3 to a high temperature approximate to the heat treatment temperature in region 50. Owing to the construction for preventing the contact of the hydrogen gas with the vitreous silica, the silicon etching is prevented or reduced significantly.

[0073] The hydrogen gas is not brought into contact with furnace tube 32 in the high temperature region in the upstream side from wafer W. The wording "high temperature region in the upstream side from wafer W" herein means a portion of hydrogen gas flow upstream relative to wafer W, and is heated to a high temperature by heater 3. This region is not present in the apparatus of Fig. 3. This region is present in the embodiment of Fig. 1, including the portion of gas introduction pipe 33 in region 50. In Fig. 3, gas introduction pipe 33 is not included in the high temperature region since it is not heated by heater 3 and the temperature rise is less even though it is placed at the upstream position.

[0074] In this embodiment, the hydrogen gas is not brought into contact with the vitreous silica at the high temperature region in the upstream portion of the gas flow. Thereby, arrival of the released metallic impurity and water formed from the vitreous silica into the hydrogen gas at wafer W is prevented, and the metal contamination and silicon etching cause by the hydrogen gas is prevented or reduced greatly.

(Embodiment 3)

[0075] A third embodiment of the present invention is described by reference to Fig. 4. In this embodiment, gas inlet 5 is provided at the bottom end portion of inner tube 31, and is formed in one body with inner-tube mount 22. The numeral 35 indicates a hole for gas vent at the top end of inner tube 31.

[0076] In hydrogen annealing of wafer W at a temperature, for example, of 1000°C or higher, the hydrogen gas is introduced from gas inlet 5 at the bottom end of inner tube 31, allowed to flow upward in inner tube 31, and then introduced through hole 35 at the top of inner tube 31 into furnace tube 32. Subsequently, the hydrogen gas is allowed to flow downward through the interspace between furnace tube 32 and inner tube 31, and is discharged from vent 6 at the bottom end of furnace tube 32.

[0077] In this embodiment, the same effects are achieved as in Embodiment 2. Further, the arrangement of the hydrogen introduction portion and the hydrogen discharge portion shown in Fig. 4 eliminates stagnation of hydrogen flow, enabling rapid gas substitution.

[0078] Further in this embodiment, the hydrogen gas is introduced and discharged as described above. Therefore, gas inlet 5 and gas vent 6 can be placed both at lower portion of the apparatus, which facilitates connection with external pipings and inspection of the connection.

[0079] Heat barrier 9 is constituted of vitreous glass such as foamed quartz. The hydrogen gas fed through flow path 41 in contact with heat barrier 9 to wafer W. Since the heat barrier is at the outside of high temperature region 50, moisture is not produced there, so that the etching is prevented.

(Embodiment 4)

[0080] A fourth embodiment of the present invention is described below by reference to Fig. 5.

[0081] At gas outlet hole 35, a check valve is provided which comprises projection 36 formed at the periphery of hole 35, and cap 37 to cover outlet hole 35. Projection 36 is formed from SiC in one body with inner tube 31. Cap 37 is also made of SiC. The gas pressure in inner tube 31 pushes up cap 37 to give a gap at gas outlet hole 35 to allow hydrogen gas to flow from inner tube 31 through this gap to interspace 42 between inner tube 31 and furnace tube 32. The back flow of the gas is stopped by the check valve. Projection 36 keeps cap 37 not to come off from outlet hole 35.

[0082] The check valve stops a back flow of the metal impurity which is released from the fused quartz of furnace tube 32 and moisture which is formed by contact of hydrogen gas with the fused quartz of furnace tube 32 into inner tube 31, and prevents or reduces remarkably the metal contamination and the etching of the silicon.

[0083] In this embodiment, as described above, a back flow checking means is provided which checks a back flow the hydrogen gas from the space between furnace tube 32 and inner tube 31 into inner tube 31. The back flow checking means may be the above check valve, but is not limited thereto. For example, the means may be a simple orifice in the gas flow path.

(Embodiment 5)

[0084] Fig. 6 shows the heat treatment apparatus of this embodiment of the present invention. This heat treatment apparatus comprises inner tube 31 having an inside face comprised of non-silicon oxide like SiC, furnace tube 32 made of vitreous silica like fused quartz, and mantle tube 45 having a surface comprised of non-silicon oxide like SiC. The numerals 24, 25, and 47 respectively indicate an O-ring, and the numeral 48 indicates a flange.

[0085] The hydrogen-containing reducing gas is introduced from gas inlet 5 at the bottom through flow path 41 into the space enclosing wafer W. The gas is further allowed to flow through hole 35, and check valve (36,37) to flow path 42 between furnace tube 32 and inner tube 31, and is discharged from vent 6. Interspace 43 between furnace tube 32 and closed mantle tube 45 is purged with an inert gas such as He, Ar, Ne, N₂, Kr, and Xe which is introduced from purge gas inlet 46 at the bottom and is discharged from purge gas vent 44 at the top.

[0086] The hydrogen gas is not brought into contact with silicon oxide heated at a temperature of 1000°C or higher, before the gas is introduced into the space which encloses wafer W. Specifically, since heat barrier 9 made of foamed quartz is placed at the outside of high-temperature heating region 50 heated by heater 3, the hydrogen gas flowing through flow path 41 does not cause moisture generation, therefore the moisture in the hydrogen gas being negligible.

[0087] The space in inner tube 31 and in high-temperature heating region 50, namely the space enclosing the wafer is surrounded by inside face comprised of a non-silicon material like SiC entirely, where the moisture is not generated. The gas flow is kept uniform in inner tube 31 by discharging the gas from hole 35 at the center of the top of the tube. Furnace tube 32, which is a closed tube made of silicon oxide like fused quartz, exhibits a high heat-insulation effect, uniformizing the temperature in high-temperature heating region 50. Even if hydrogen leaks out of inner tube 31, it will not leak out of furnace tube 32. Boat 4 for holding wafer W has also a surface made of non-silicon oxide like SiC, not producing moisture.

[0088] The closed mantle tube 45 and the purge gas prevent penetration of metal impurity from heater 3 into inside tubes.

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(Heat Treatment)

[0089] The heat treatment is conducted in Embodiments 1 to 5 of the present invention as described below.

[0090] A semiconductor article like an Si wafer is placed in inner tube 32 in the apparatus shown in any of Fig. 1, Figs. 3 to 6. A hydrogen-containing gas is introduced into inner tube 32 to keep the semiconductor article in a reducing atmosphere. Before or after the start of introduction of the hydrogen-containing gas, the semiconductor article is heated up to a prescribed temperature. The heat treatment temperature is preferably not lower than 900°C but lower than the melting point of silicon, more preferably in the range from 1000 to 1200°C. The heat treatment time depends on the intended annealing effect, and is usually selected suitably in the range from 3 minutes to 5 hours. Thus heat treatment of the semiconductor article is completed.

[0091] The semiconductor article employed in the present invention includes CZ Si wafer, SOI Si wafer, and wafers having an Si film or Si islands on a vitreous silica. The wafer may be of any state, taken before, in, or after a semiconductor production process. In particular, the present invention is effective in hydrogen-annealing of an SOI wafer having an unpolished rough surface.

[0092] The treatment gas employed in the present invention is 100% hydrogen or a mixture containing 1% to 99% hydrogen and an inert gas.

[0093] The pressure of the hydrogen-containing reducing atmosphere may be a higher pressure, an ordinary pressure, or a reduced pressure. Preferably the pressure ranges from 1.02×10^5 Pa to 1.33 Pa, more preferably from 1.02×10^5 Pa to 1.33×10^3 Pa.

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(Process for Producing Semiconductor Article)

[0094] A process is described below for producing a semiconductor article by a heat treatment method of the present invention.

[0095] Fig. 7 is a flow chart of production of a bonding SOI substrate typified by a hydrogen injection peeling method, a PACE method, and epitaxial layer transfer method.

[0096] In Step S1, a first base member is provided. An example of the first base member is provided by injecting hydrogen ions or rare earth gas ions into an Si wafer having insulation layer formed by oxidation at least on one face to form a separation layer (latent layer) at a prescribed depth. Another example thereof is prepared by making porous a surface of an Si wafer and growing epitaxially thereon a nonporous Si layer. In a PACE method, the first base member is an Si wafer having no oxide film, or having an oxidized surface.

[0097] In Step S2, a second base member is provided. Example of the second base member includes usual Si wafers, Si wafers having an oxidized surface, Si wafers having a natural oxide film eliminated, quartz wafers, and metal

base plates.

[0098] In Step S3, the first base member and the second base member provided above are bonded directly or indirectly with interposition of an adhesive layer. In this step, at least one of the bonding faces of the first base member and the second base member should have an insulation layer. In production of a base member having a structure of other than SOI, the insulation layer is not always necessary. The bonding face may be activated by irradiation with ions of hydrogen, oxygen, nitrogen, or a rare earth gas.

[0099] In Step S4, a part (unnecessary portion) of the first base member is removed from the assembly of the bonded first and second base members. The methods of the removal are classified roughly into two. In a first method, a part of the first base member is removed from the back face thereof by grinding, etching, or a like technique. In a second method, the surface portion and the inner portion of the first base member are separated at the separation layer formed preliminarily in the first base member. By the second method, the separated unnecessary portion keeps the shape of the wafer, so that it can be reused as the first base member or the second base member. The separation can be conducted by exfoliation by heat treatment, or blowing a fluid comprised of a liquid or a gas against the lateral side of the assembly, or by mechanical peeling.

[0100] The assembly (SOI substrate) having the unnecessary portion removed has a rough surface with voids formed by ion injection, pores of the porous layer, or projections and cavities caused by grinding or etching. Therefore, in Step S5, the rough upper layer of the silicon layer is smoothened by conducting hydrogen annealing with the above-described heat treatment apparatus. Thereby, the etched silicon layer surface is smoothened to a surface roughness of not more than 0.2 nm (1 μ m square). By optimizing the smoothening conditions, the roughness can be reduced to be not more than 0.15 nm, or further not more than 0.1 nm.

[0101] Next, a process is described below in detail for producing a semiconductor substrate according to an epitaxial layer transfer method by reference to Figs. 8A to 8F.

[0102] In Step S31 of Fig. 8A, base plate 131 comprised of Si single crystal is provided as the first base member, and thereon a porous structure layer 133 is formed at least at the main surface side. The porous Si can be formed by anodization of an Si base plate in an HF solution. The porous layer has a structure like a sponge in which pores of about 10^1 nm to about 10 nm in diameter are formed at an intervals of about 10^1 nm to about 10 nm. The density can be controlled in the range from 2.1 to 0.6 g/cm³, in comparison with the density 2.33 g/cm³ of single crystal Si, by changing the concentration of the HF solution in the range of 50% to 20%, changing the alcohol addition ratio, or changing the electric current density. The porosity of the porous portion can be changed by adjusting preliminarily the resistivity and the electric conduction type. In the p-type, a non-degenerated base plate (P⁻) forms pores of smaller diameter and the pores density of higher by one digit in comparison with a degenerated base plate (P⁺) under the same anodization conditions, and the porosity is higher. Thus, the porosity can be controlled by controlling the pore forming conditions without limiting the control method. Porous layer 133 may be a single layer or a lamination of layers of different porosities. The porosity can be raised by ion implantation to reach the porous layer, whereby bubbles are formed on the pore walls of the porous layer near the implantation. The ion implantation may be conducted before, or after the formation of the porous layer by anodization, or after formation of a single crystal semiconductor layer structure on porous layer 133.

[0103] In the following Step S32 of Fig. 8B, at least one nonporous single crystal semiconductor layer 123 is formed on porous layer 133. Nonporous single crystal semiconductor layer 123 may be selected suitably from epitaxially grown single crystal Si layers, layers formed by making the surface layer of porous layer 133 nonporous, or the like. On the single crystal Si layer 123, silicon oxide layer 122 is formed by thermal oxidation. Thereby, the interface level between the single crystal silicon layer and the embedded oxide layer is made lower.

[0104] In Step S33 of Fig. 8C, the main face (bonding face) of the above semiconductor base plate having nonporous single crystal Si layer 123 is brought into close contact with a surface (bonding face) of second base plate 121. Before the contact, adhering matters and foreign matters are preferably removed by washing. The second base plate may be selected from Si plates having an Si oxide film thereon, light-transmissive plates like quartz plates, sapphire plates, and the like, but is not limited thereto. Any material having a flat and smooth bonding surface may be used as the second base plate. In Fig. 8C, the first base plate and the second base plate are bonded with interposition of insulation layer 122. However, insulation layer 122 is not essential. In the bonding, an insulating thin plate may be placed between the first base plate and the second base plate.

[0105] In the next step, the unnecessary back face portion of the first base plate 131 and porous layer 133 are removed to bare nonporous single crystal Si layer 123. This removal can be conducted in two alternative methods, but is not limited thereto.

[0106] In a first method, first base plate 131 is removed from back side to bare porous layer 133 (Step S34 of Fig. 8D). Then, porous layer 133 is removed to bare nonporous silicon layer 123 (Step S35 of Fig. 8E). The removal of the porous layer is preferably conducted by selective etching. By use of an etching solution containing hydrofluoric acid at least and aqueous hydrogen peroxide, the porous silicon can be etched selectively relative to nonporous single crystal silicon by a selectivity factor of 10^5 . A surfactant may be added to the etching solution to prevent bubble adhering.

An alcohol such as ethanol is added thereto suitably. If the porous layer is thin, the selective etching may be omitted.

[0107] In a second method, the base plates are separated at porous layer 133 as the separation layer to obtain the state of the base plate as shown in Step S34 of Fig. 8D. The method of the separation includes application of external mechanical force such as pressing, pulling, shearing, and wedging; application of ultrasonic wave; heating; oxidation to swell the porous Si from the periphery to apply internal pressure to inside porous Si; application of heat pulse to cause thermal stress or softening; and ejection of a fluid such as water jet, and gas jet, but is not limited thereto.

[0108] In next Step S35, the unremoved remaining portion of porous layer 133 is removed from the surface of second base plate 121 by etching in a similar manner as the etching of the porous layer. If the remaining portion of porous silicon 133 on second base plate 121 is very thin and uniform in thickness, the wet etching of the porous layer with hydrofluoric acid and hydrogen peroxide may be omitted.

[0109] In Step S36 of Fig. 8F, single crystal Si layer 123 is heat-treated to smoothen the rough surface by heat treatment in a hydrogen-containing reducing atmosphere by means of any of the apparatuses shown in Fig. 1, and Figs. 3 to 6.

[0110] The semiconductor base plate prepared according to the present invention has single crystal Si film 123 formed in a flat uniform thin film on second base plate 121 with interposition of insulation layer 122 in a large area over the entire base plate. Such a semiconductor base plate is suitable for preparing insulated electronic elements.

[0111] Separated first single crystal Si base plate 131 can be reused, after removal of the remaining porous layer on the base plate separation face and, if the surface is intolerably rough, subsequent surface-smoothening, as first single crystal base plate 131 or second base plate 121.

20 (Example 1)

[0112] A silicon wafer of 5 inches in diameter was treated for hydrogen annealing under conditions of the heat treatment temperature of 1100°C, the heat treatment time of 4 hours, and the hydrogen gas flow rate of 10 L/min. The hydrogen treatment was conducted, for comparison, by use of the apparatus shown in Fig. 2, and by use of the apparatus shown in Fig. 1 to confirm the effect of reduction of metal contamination of the present invention. Inner tube 31 employed was made of a silicon carbide material having a SiC coating layer formed by CVD. The metal contamination by the respective apparatuses was compared by measurement of the carrier life time of the wafers after the heat treatment. Table 1 shows the results. In the heat treatment according to the present invention, the carrier life was improved by a factor of about 2 in comparison with the conventional heat treatment as shown in Table 1, which shows the effects of reducing the metal contamination of the wafer in hydrogen annealing.

Table 1

	Heat treatment apparatus	
	(Fig. 1)	(Fig. 2)
Carrier life time (μsec)	15	28

40 (Example 2)

[0113] A surface of a 8-inch boron-doped (100) Si wafer having resistivity of 0.017 Ωcm was anodized in a 2:1 mixture of 49% HF and ethyl alcohol to form a porous silicon layer in a thickness of 10 μm on the surface of the wafer. This silicon wafer was heat-treated in an oxygen atmosphere at 400°C for one hour to form a thin oxide film on the surface of the pores. Then, from the external face of the porous layer and vicinity thereof, the formed oxide film was removed by immersion in an aqueous 1.25% HF solution for 30 seconds. The wafer was washed sufficiently with water, and dried. This silicon wafer was heat-treated in an epitaxial growth apparatus with introduction of a trace amount of a silane gas in a hydrogen atmosphere at 1100°C to close nearly all of the holes on the external face of the porous silicon. Subsequently, a single crystal Si film was formed in an average thickness of 310 nm ± 5 nm on the porous silicon by addition of dichlorosilane or silane to the hydrogen gas. This silicon wafer was transferred from the epitaxial growth apparatus to an oxidation furnace, and the surface of the single crystal Si film was oxidized by hydrogen-oxygen combustion gas to form a silicon oxide film in a thickness of 200 nm. As the result of the oxidation, the thickness of the single crystal silicon film decreased to 210 nm. This silicon wafer and a separately provided second silicon wafer were washed by a conventional wet washing process for silicon devices to clean the surfaces, and the two wafers were bonded together. The resulting silicon wafer assembly was heat-treated in an oxygen-containing atmosphere at 1100°C for one hour to strengthen the bonding of the wafers. In this heat treatment, the temperature was elevated in an atmosphere of nitrogen-oxygen mixture, kept at 1100°C in oxygen atmosphere for one hour, and lowered in a nitrogen atmosphere. The non-bonded face of the first wafer was ground to bare the porous silicon. Then the porous silicon

was removed by etching by immersion in a mixed solution of hydrofluoric acid and aqueous hydrogen peroxide. After washing, the wafer was washed sufficiently by wet washing. Consequently, the single crystal silicon film was transferred together with the silicon oxide onto the second silicon wafer to produce an SOI wafer.

[0114] The thickness of the transferred single crystal silicon was measured at 10 mm lattice points in the plane. The average thickness was 210 nm with variation of ± 7 nm. The surface roughness was measured with atomic force microscopy in the range of 1 μm square and 50 μm square at 256 x 256 points. The surface roughness was 10.1 nm, and 9.8 nm respectively in terms of average square roughness R_{rms}. The boron concentration in single crystal silicon film was $1.2 \times 10^{18}/\text{cm}^3$ according to secondary ion mass spectroscopy (SIMS).

[0115] The plural SOI wafers produced as described above, after removal of the silicon oxide films of the back faces by hydrofluoric acid etching, were placed in a heat treatment apparatus as shown in Fig. 1. The wafers were set horizontally with intervals of 6 mm between the silicon of the back face of one SOI wafer and the surface SOI layer of the adjacent SOI wafer with the centers of the wafers positioned on the center line of the furnace tube on a boat made of SiC. Above the uppermost SOI wafer, a commercial silicon wafer was set at the same interval. The atmosphere in the furnace was substituted with hydrogen. The temperature in the furnace was elevated to 1100°C, kept for 4 hours, and then lowered. The thickness of the SOI layers measured again.

[0116] For comparison, the SOI wafers prepared in the same manner was hydrogen-annealed with an apparatus as shown in Fig. 2.

[0117] As shown in Table 2, the maximum etching amount is less in the present invention by a factor of 1/8 than the conventional method, and correspondingly the variation of the etching is greatly decreased. Obviously, the present invention provides an SOI base plate with decreased etching and uniform thickness.

Table 2

	Heat treatment apparatus	
	(Fig. 2)	(Fig. 1)
Maximum etching (nm)	8	1
Minimum etching (nm)	1	0

[0118] As described above, the present invention provides a heat treatment apparatus which does not cause metal contamination of an wafer by silicon oxide of a furnace tube as the contamination source and does not cause etching of a silicon wafer body by moisture formed with the reaction of silicon oxide and the hydrogen gas. The present invention also provide a process of heat treatment employing the above heat treatment apparatus. Semiconductor article having excellent properties can be produced according to the process of the present invention.

Claims

1. A heat treatment apparatus comprising a first tube, a second tube placed therein, and a heater, wherein the first tube is tightly closable and is made of vitreous silica having an impact strength higher than that of the second tube, the second tube has at least an internal face comprised of non-silicon oxide, and a gas flow path is constructed to introduce a gas into a treatment space in the second tube without passing over a face comprised of silicon oxide heated to a high temperature by the heater.
2. The heat treatment apparatus according to claim 1, wherein the vitreous silica is fused silica, and the non-silicon oxide is silicon carbide.
3. The heat treatment apparatus according to claim 1, wherein the non-silicon oxide is selected from the group consisting of silicon, silicon carbide, silicon nitride, aluminum oxide, and boron nitride.
4. The heat treatment apparatus according to claim 1, wherein the second tube has a surface coated with a silicon carbide film.
5. The heat treatment apparatus according to claim 1, wherein the face comprised of non-silicon oxide is heated at a temperature of 900°C or higher.
6. The heat treatment apparatus according to claim 1, wherein the face comprised of non-silicon oxide is heated at a temperature of 1000°C or higher.

7. The heat treatment apparatus according to claim 1, wherein the gas is hydrogen gas and introduced together with or without an inert gas into the second tube.

5 8. The heat treatment apparatus according to claim 1, wherein the second tube is extended to upstream side of the treatment space.

10 9. The heat treatment apparatus according to claim 1, wherein the gas is hydrogen gas, and an inlet for the hydrogen gas into the second tube is provided outside the treatment space, and a vent for hydrogen gas from the second tube is provided outside the treatment space and reverse to the inlet.

15 10. The heat treatment apparatus according to claim 9, wherein the gas outlet is open to the inside of the first tube, and a vent is provided on the first tube to flow the hydrogen gas through the inside space for discharging the hydrogen gas.

20 11. The heat treatment apparatus according to claim 9, wherein a flow preventing means is provided at the discharge portion to prevent a flow of the gas from the first tube to the second tube.

12. The heat treatment apparatus according to claim 1, wherein a third tube is provided between the first tube and the heater.

25 13. The heat treatment apparatus according to claim 12, wherein the third tube is tightly closable.

14. The heat treatment apparatus according to claim 12, wherein the surface at least of the third tube is comprised of non-silicon oxide.

30 15. The heat treatment apparatus according to claim 12, wherein the third tube is made of silicon carbide.

16. The heat treatment apparatus according to claim 12, wherein a purge gas is introduced into an interspace between the third tube and the first tube.

35 17. The heat treatment apparatus according to claim 12, wherein the second tube and the third tube are both closable tightly.

18. The heat treatment apparatus according to claim 1, wherein a support having a non-silicon oxide surface and a heat barrier having a silicon oxide surface are placed in the second tube.

40 19. The heat treatment apparatus according to claim 1, wherein the heater is provided above the heat barrier placed in the second tube.

20. The heat treatment apparatus according to claim 1, wherein the gas is hydrogen gas, and the hydrogen gas is introduced from a lower portion of the second tube, and is discharged from a lower portion of the first tube.

45 21. The heat treatment apparatus according to claim 1, wherein a purge gas is introduced from the outside through the bottom of the first tube, and is discharged from the outside through the top of the first tube.

22. A heat treatment apparatus comprising a first tube, a second tube placed therein, and a heater, wherein a gas inlet for introducing the gas in the second tube is provided below the heater, a hole for communicating the second tube to the first tube is provided at a top portion of the second tube, a vent is provided at a bottom portion of the first tube for discharging the gas from inside of the first tube, the first tube is constructed from fused quartz and is closable, the second tube has a non-silicon oxide surface and is closable, and the heater is provided at a higher level than a heat barrier placed in the second tube.

50 23. The heat treatment apparatus according to claim 22, wherein a closable third tube having a non-silicon oxide surface is provided outside the first tube, a purge gas inlet is provided at a bottom portion of the third tube, and a purge gas vent is provided at a top portion of the third tube.

55 24. The heat treatment apparatus according to claim 22, wherein the heat barrier comprises foamed quartz.

25. The heat treatment apparatus according to claim 22, wherein the heat barrier is not heated to 1000°C or higher.

26. A heat treatment process for heat-treating a semiconductor article by means of the heat treatment apparatus set forth in claim 1.

5 27. The heat treatment process according to claim 26, wherein the semiconductor article has a silicon body.

28. The heat treatment process according to claim 26, wherein the semiconductor article is heat-treated in a hydrogen containing reducing atmosphere at a temperature not lower than 900°C.

10 29. The heat treatment process according to claim 28, wherein the semiconductor article is heat-treated at a temperature not lower than 1000°C.

30. The heat treatment process according to claim 27, wherein the semiconductor article is an SOI substrate.

15 31. The heat treatment process according to claim 30, wherein the semiconductor article is a bonding SOI substrate.

32. A heat treatment process for heat-treating a semiconductor article by means of the heat treatment apparatus set forth in claim 22.

20 33. The heat treatment process according to claim 32, wherein the semiconductor article has a silicon body.

34. The heat treatment process according to claim 32, wherein the semiconductor article is heat-treated in a hydrogen containing reducing atmosphere at a temperature not lower than 900°C.

25 35. The heat treatment process according to claim 34, wherein the semiconductor article is heat-treated at a temperature not lower than 1000°C.

36. The heat treatment process according to claim 33, wherein the semiconductor article is an SOI substrate.

30 37. The heat treatment process according to claim 36, wherein the semiconductor article is a bonding SOI substrate.

38. A process for producing a semiconductor article comprising bonding a first base plate and a second base plate, removing an unnecessary portion of the first base plate from the second base plate, and heat-treating a silicon body on the second base plate in a hydrogen-containing reducing atmosphere by means of the heat treatment apparatus according to claim 1.

35 39. The process according to claim 38, wherein a separation layer is formed in the first base plate, and the unnecessary portion is removed by separation at the separation layer.

40 40. The process according to claim 38, wherein the unnecessary portion of the first base plate is removed by any of methods of polishing, grinding, and etching.

45 41. The process according to claim 38, wherein the silicon body is an epitaxial layer.

42. The process according to claim 38, wherein the process comprises forming a porous layer on a main face of the first silicon single crystal base plate, forming a single crystal silicon layer on the porous layer, bonding the main face of the silicon single crystal base plate to the surface of the second base plate, and removing the porous layer to bare the single crystal silicon layer.

50 43. A process for producing a semiconductor article comprising bonding a first base plate and a second base plate, removing an unnecessary portion of the first base plate from the second base plate, and heat-treating a silicon body on the second base plate in a hydrogen-containing reducing atmosphere by means of the heat treatment apparatus according to claim 22.

55 44. The process according to claim 43, wherein a separation layer is formed in the first base plate, and the unnecessary portion is removed by separation at the separation layer.

45. The process according to claim 43, wherein the unnecessary portion of the first base plate is removed by any of methods of polishing, grinding, and etching.

46. The process according to claim 43, wherein the silicon body is an epitaxial layer.

5 47. The process according to claim 43, wherein the process comprises forming a porous layer on a main face of the first silicon single crystal base plate, forming a single crystal silicon layer on the porous layer, bonding the main face of the silicon single crystal base plate to the surface of the second base plate, and removing the porous layer to bare the single crystal silicon layer.

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FIG. 1

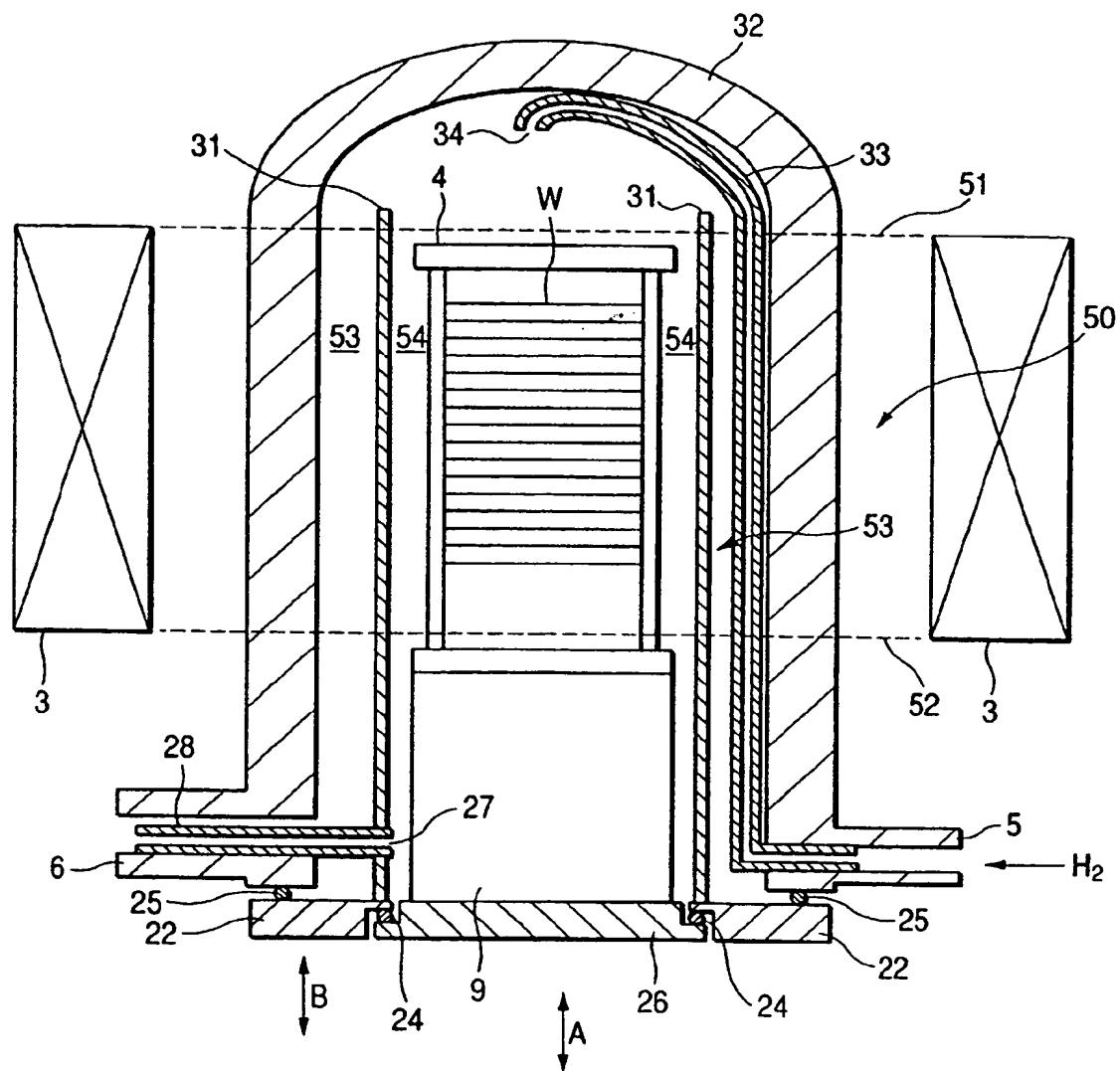


FIG. 2

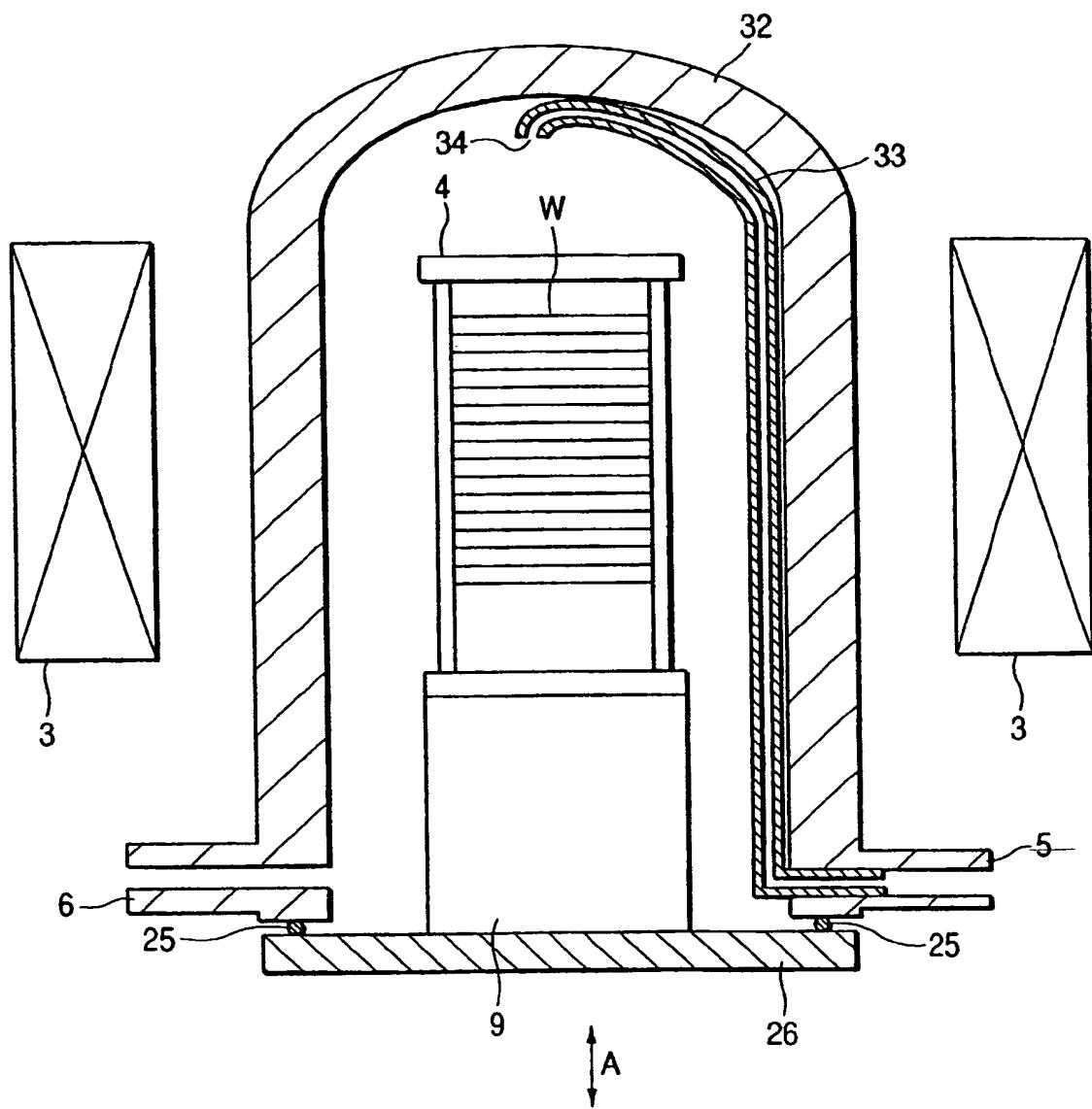


FIG. 3

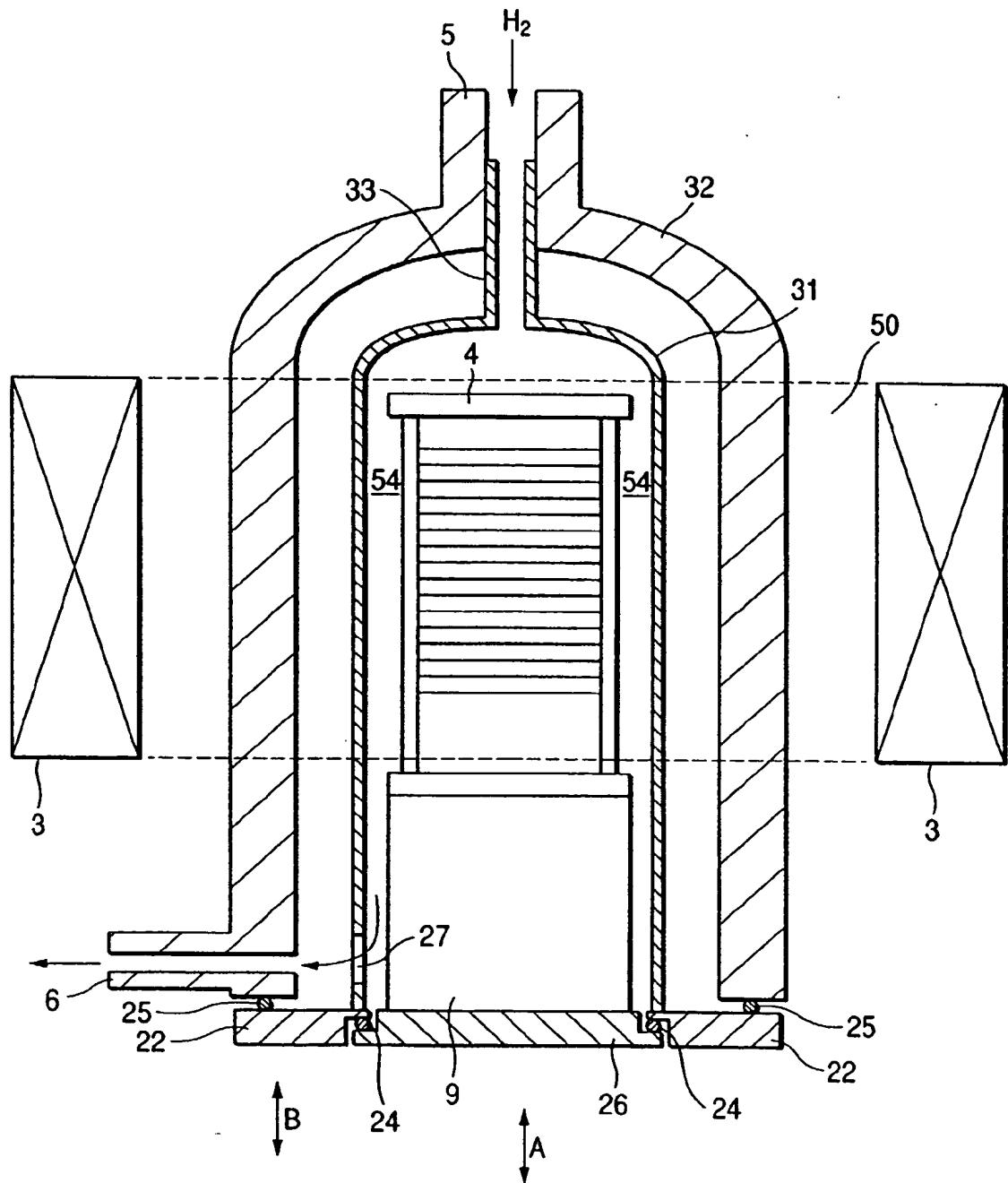


FIG. 4

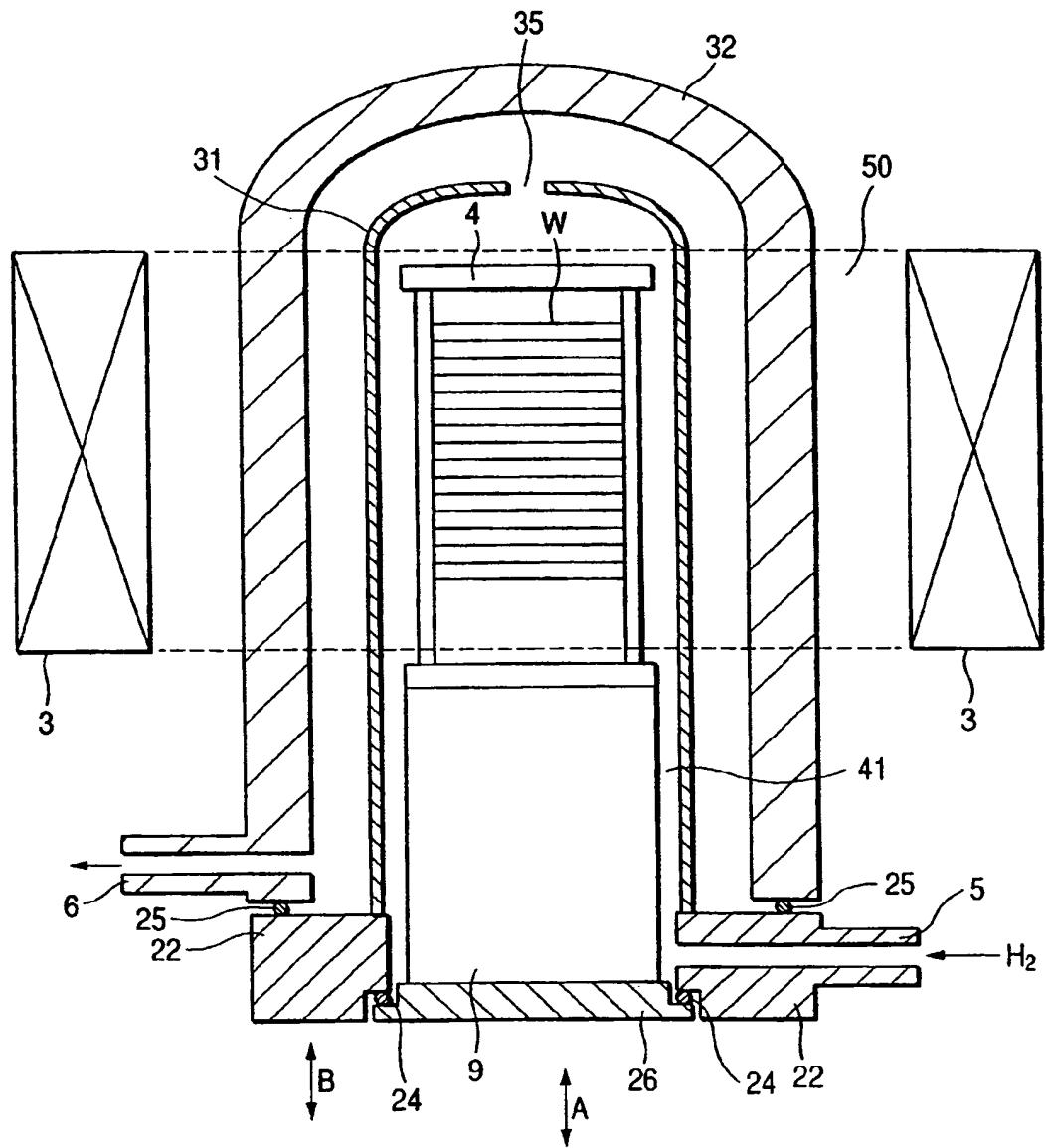


FIG. 5

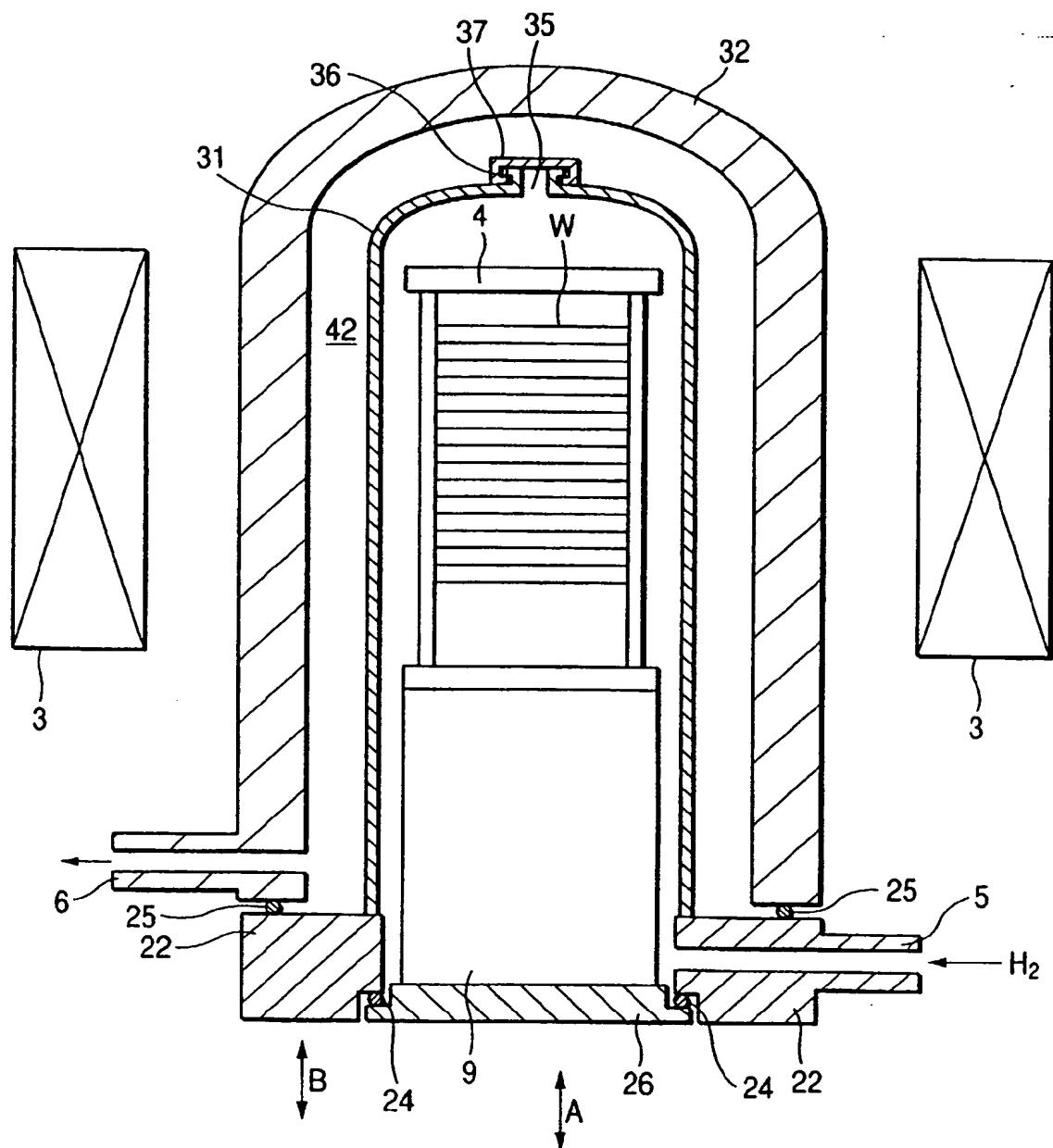


FIG. 6

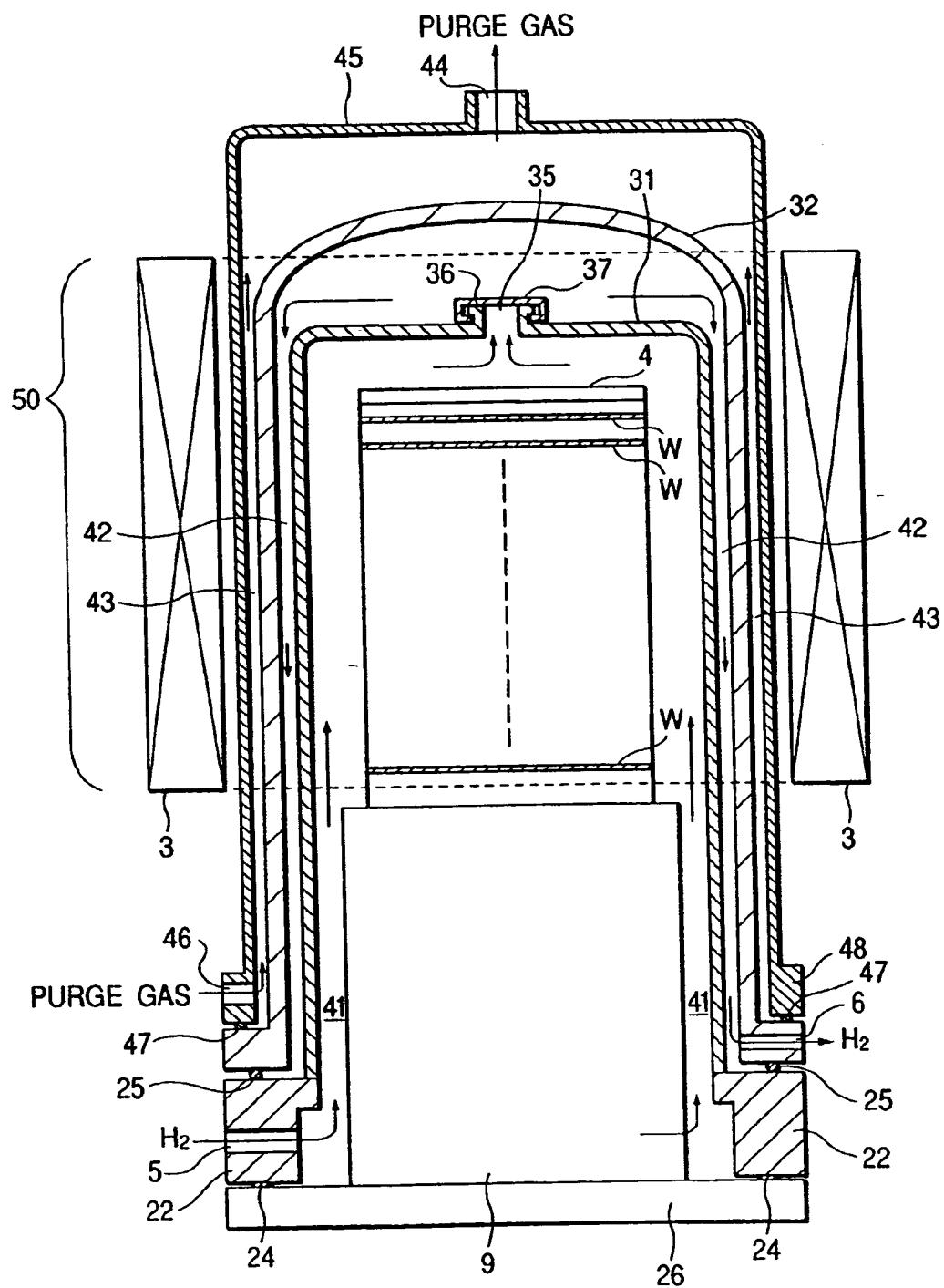
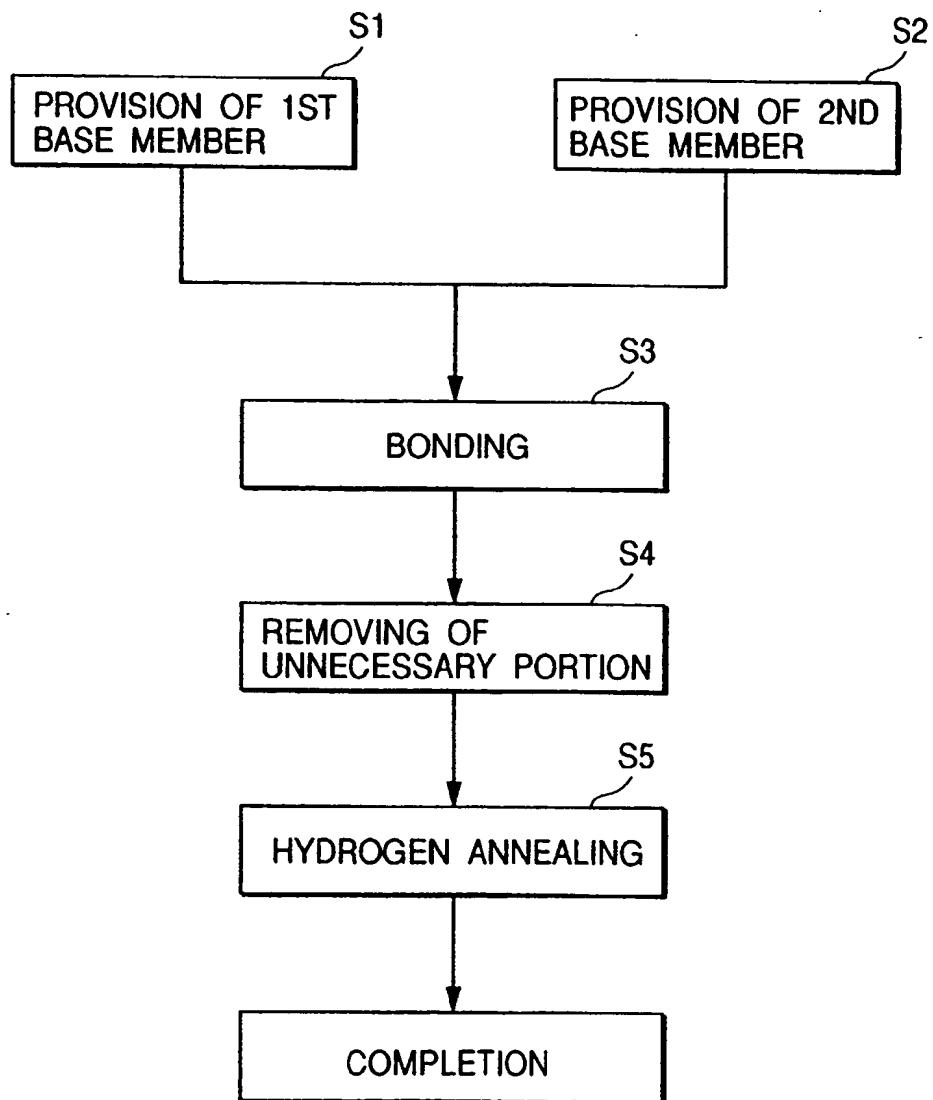


FIG. 7



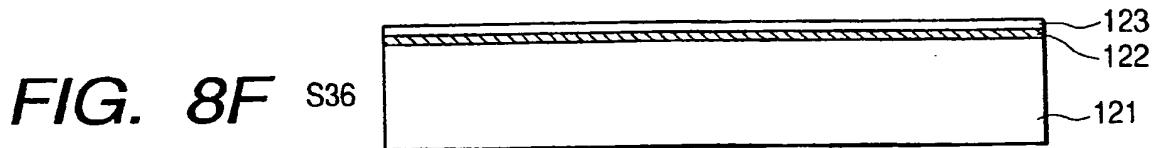
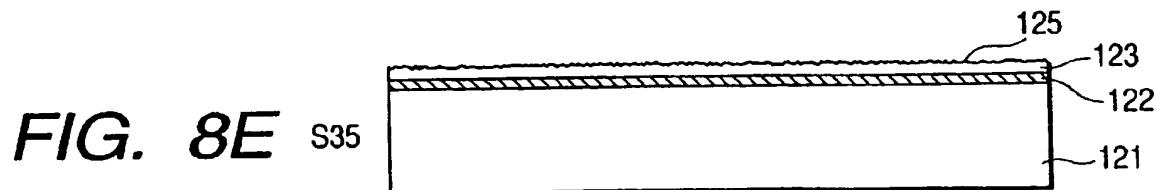
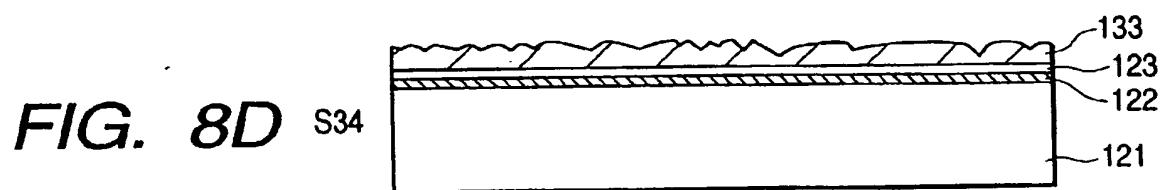
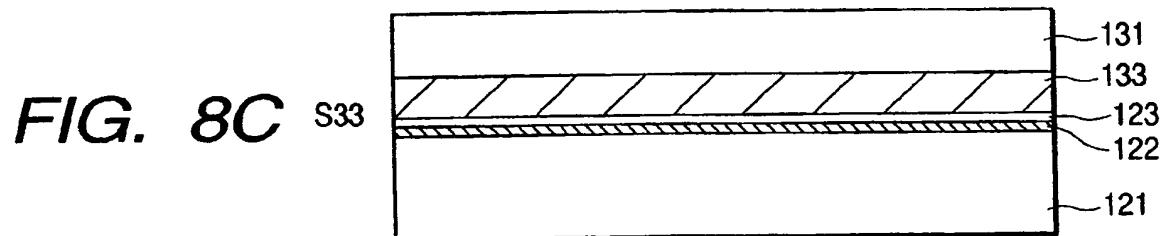
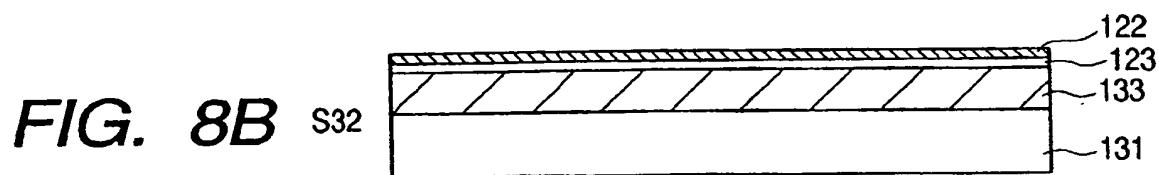


FIG. 9
PRIOR ART

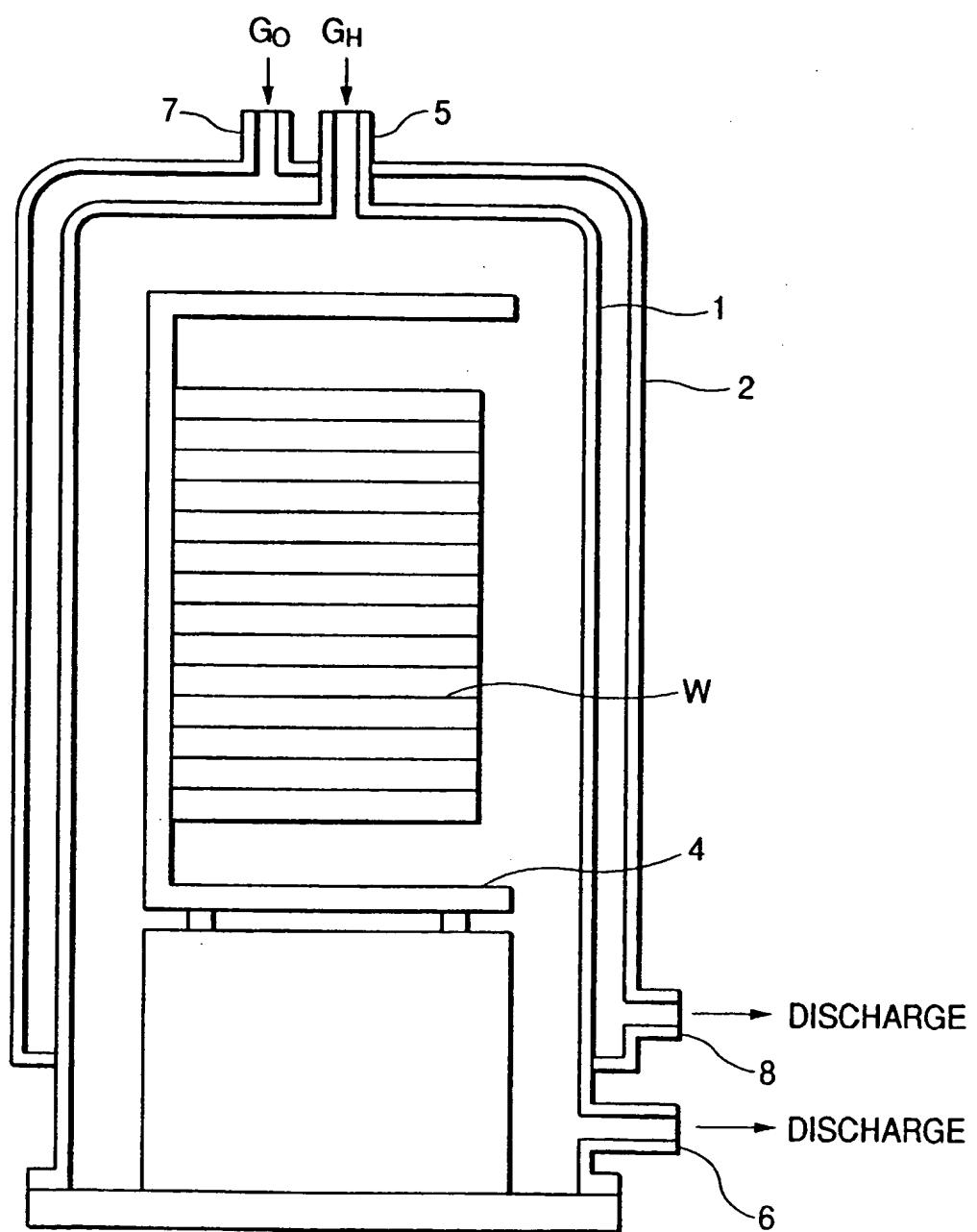


FIG. 10
PRIOR ART

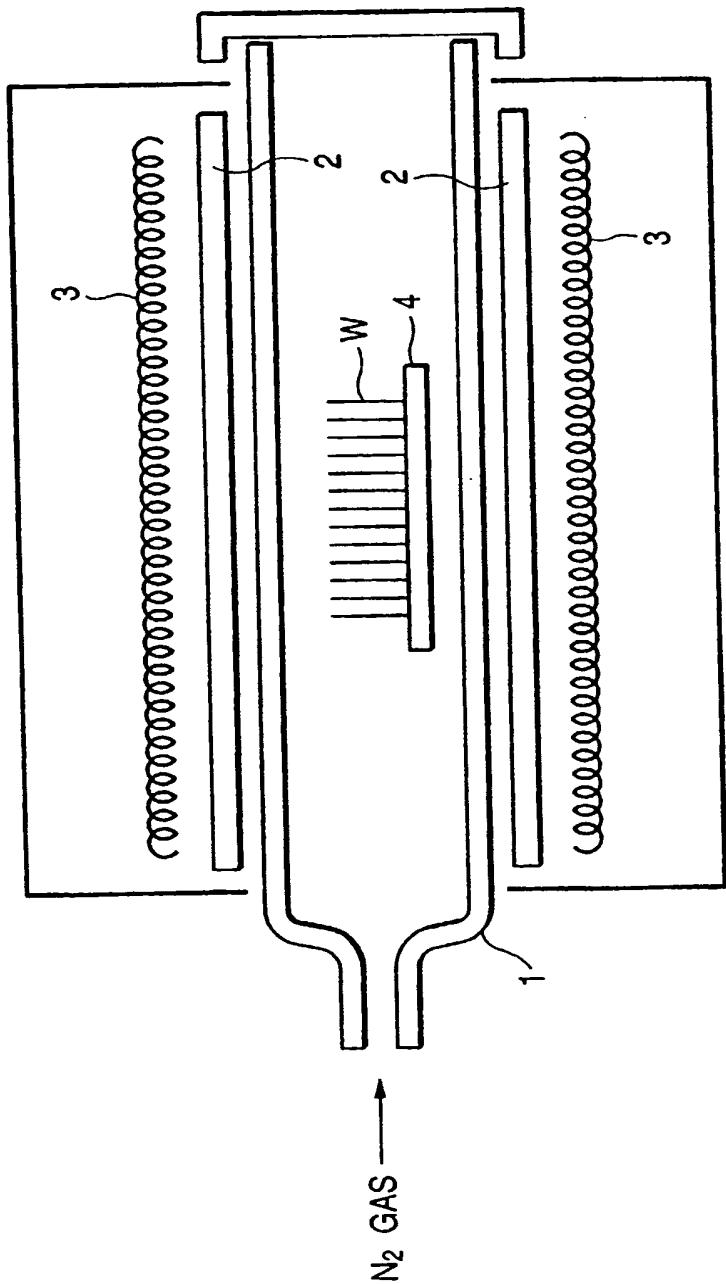


FIG. 11
PRIOR ART

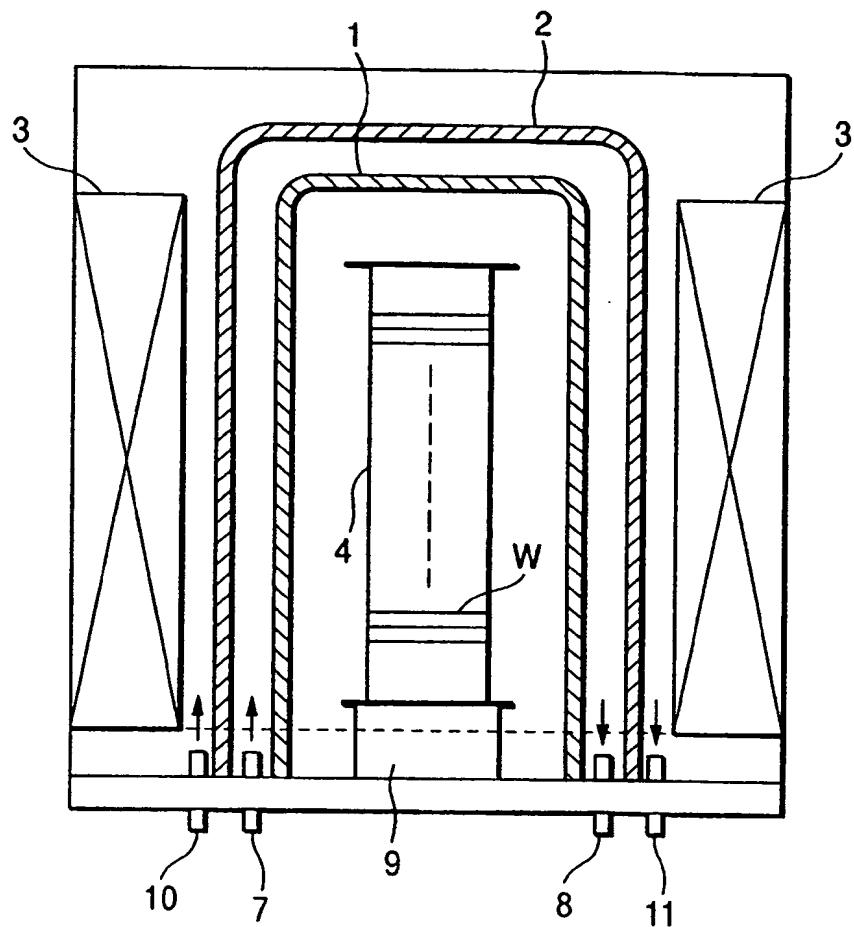


FIG. 12
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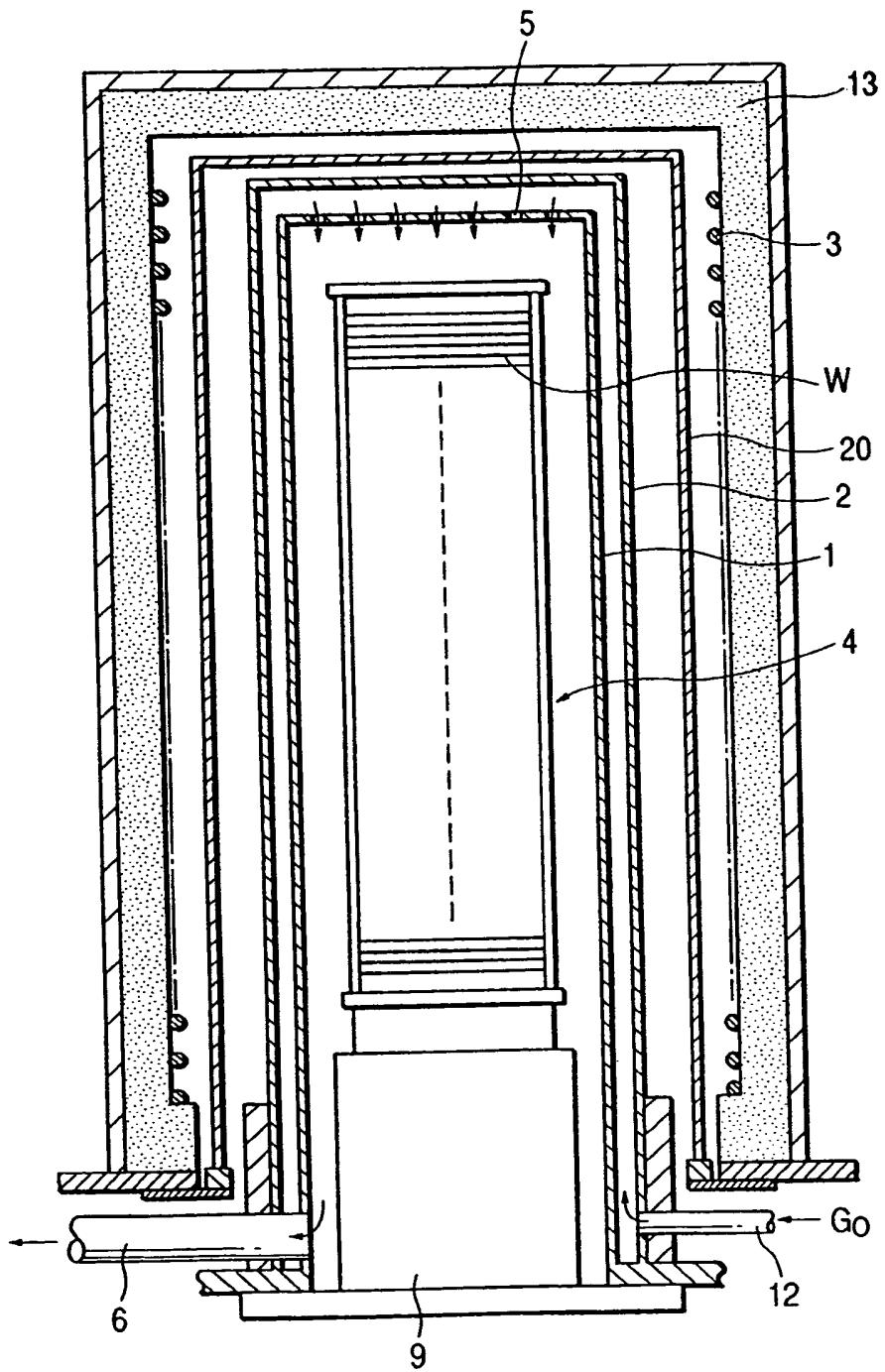
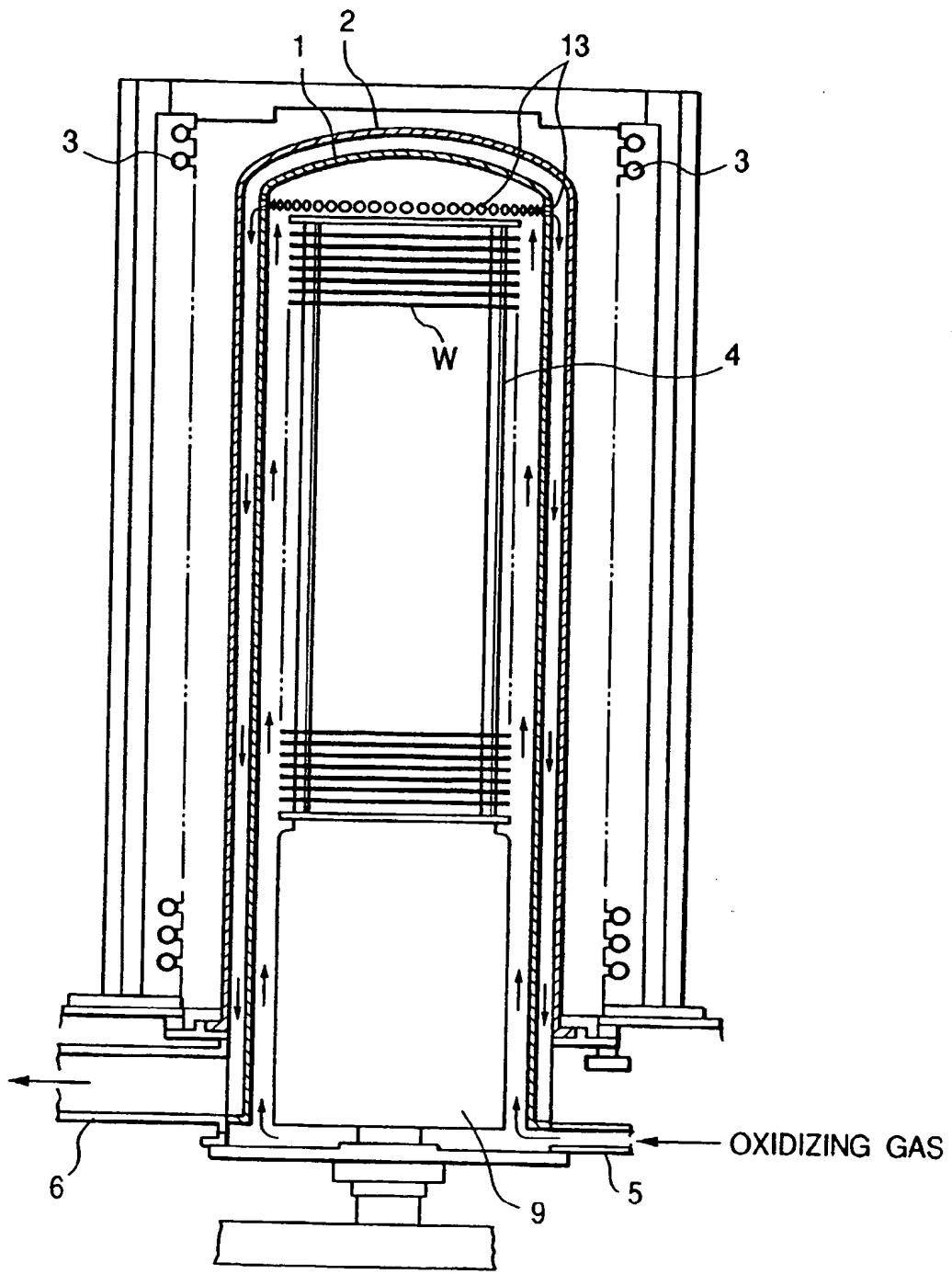


FIG. 13
PRIOR ART



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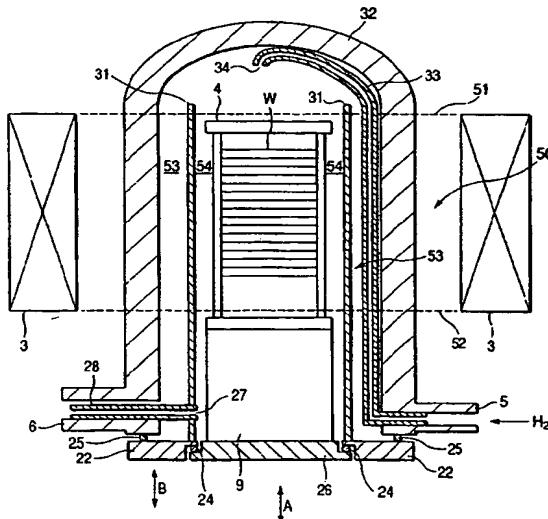
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(54) **Heat treatment apparatus, heat treatment process employing the same, and process for producing semiconductor article**

(57) A novel heat treatment apparatus is provided which comprises a first tube, a second tube placed therein, and a heater, and heat-treats a semiconductor article in the second tube in an atmospheric gas, wherein at least an internal face of the second tube is constructed from non-silicon oxide, and the first tube is constructed from vitreous silica. Thereby, hydrogen gas is fed to a wafer without passing over a face comprised of silicon oxide heated to a high temperature. This apparatus prevents metal contamination of the wafer by fused quartz tube as the contamination source, and also prevents etching of silicon by reaction of silicon oxide and silicon.

FIG. 1





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 98 31 0680

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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
MUNICH	24 November 2003	Paisdor, B	
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EP 98 31 0680

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24-11-2003

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